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EXAMINER	
TECKLU, ISAAC TUKU	
ART UNIT	PAPER NUMBER
2192	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/700,254	SCHUMACHER ET AL.	
	Examiner	Art Unit	
	ISAAC T. TECKLU	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 May 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the appeal brief filed on 04/08/2009.

2. In view of the appeal brief filled on 04/08/2009, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options.

1. file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final).

2. initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

Response to Arguments

3. Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection. See Tabloski, Jr. et al. (US 5,999,729) and Kakivaya et al. (US 7,124,405 B1), new arts made of record.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-10, 12-14 and 16-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Tabloski, Jr. et al. (US 5,999,729).

As per claim 1, Tabloski, Jr. discloses a system of managing data utilizing one or more processors and a single operating system, (see at least e.g. FIG. 1, FIG. 2, 25 and related text) comprising:

a plurality of map components (see at least col.1:65 through col.2:1-10 "… whose component… a port component… combiner component and an adapter component…", e.g. FIG. 6A, MERGE COMPONENT 44, SPLITTER COMPONENT 42, FIG. 6B, 51 and 55 and related text), each map component having one or more ports for accepting data and for producing data (see at least col.2:5-15 "… one or more input and/or output ports…. for receiving data from another component…", e.g. FIG. 6A, 41 and related text) and each map component encapsulating a particular dataflow pattern (see at least col.2:55-65 "… executable objects associated with … components… dataflow…");

compiler tools for organizing and linking said map components using said ports into an executable dataflow application (see at least col.5:50-65 "… develop the parallel program graphically… instantiated program objects and links interconnecting respective objects to represent the flow of data…" and e.g. FIG. 2, COMPILER 34 and related text); and

an executor for creating and managing data communication among map components in the dataflow application (see at least col.10:1-15 "… data flow… generate code for the object instances in the graph…", e.g. FIG. 2, EXECUTABLE PROGRAM 23 and FIG. 7A and related text) and executing the dataflow application on said one or more processors in parallel with each map component as a separate thread of execution with data supplied to the system (see at least col.8:1-20 "… each be processed by a separate one … of the parallel computer system …", col.8:45-60 "… parallel processing… single instance of a parallel processing module can be processed in parallel on plurality of processors…" and e.g. FIG. 2, OUTPUT 24, FIG. 8, step 100 and related text).

As per claim 2, Tabloski, Jr. discloses the system of claim 1, the compiler including tools for visually creating composite components comprising other map components (see at least e.g. FIG. 3 and related text) and tools for visually assembling map components into a dataflow application (see at least col.5:50-65 "… develop the parallel program graphically… instantiated program objects and links interconnecting respective objects to represent the flow of data…", e.g. FIG. 7A and related text).

As per claim 3, Tabloski, Jr. discloses the system of claim 1, at least one map component having properties determining map component design behavior (see at least e.g. FIG. 8, PROGRAM COMPOSITION MODULE 33 PERFORMS SEMANTIC ANALYSIS TO INSURE THAT ELEMENTS OF DATAFLOW GRAPH HAVE CONSISTEN SEMANTICS 103 and related text).

As per claim 4, Tabloski, Jr. discloses the system of claim 1, at least one map component having properties that affect map component execution behavior (see at least e.g. FIG. 8, PROGRAM COMPOSITION MODULE 33 PERFORMS SYNTAX CHECK OPERATION IN CONNECTION WITH DATAFLOW GRAPH 101 and related text).

As per claim 5, Tabloski, Jr. discloses the system of claim 1, at least one of the map components comprising a composite component encapsulating a particular dataflow pattern using other map components as subcomponents (see at least FIG. 8 PROGRAM COMPOSITION MODULE 33 TRAVERSES DATA FLOW GRAPH AND GENERATES HIGH-LEVEL LANGUAGE PROGRAM CODE and col.2:55-65 "… executable objects associated with … components… dataflow…").

As per claim 6, Tabloski, Jr. discloses the system of claim 1, at least one of the map components comprising a scalar map component to process a specific data transformation (see at least e.g. FIG. 7B, 41, 42 and 44 – object 53 represents a 'scalar' map component and related text).

As per claim 7, Tabloski, Jr. discloses the system of claim 1, at least one of said ports linked to transfer specific types of data (see at least col.5:50-65 "… develop the parallel program graphically… instantiated program objects and links interconnecting respective objects to represent the flow of data…", e.g. FIG. 7A and related text).

As per claim 8, Tabloski, Jr. discloses the system of claim 1, at least one of said ports initially defined as a generic port for processing generic types of data, said generic port being later

synthesized to transfer a specific sub-type of data (see at least col.2:5-15 "… one or more input and/or output ports…. for receiving data from another component…", e.g. FIG. 6A, 41 and related text).

As per claim 9, Tabloski, Jr. discloses the system of claim 1, at least one of said ports being composite, comprising a plurality of hierarchical ports (see at least col.1:65 through col.2:1-10 "… whose component… a port component… combiner component and an adapter component…", e.g. FIG. 6A, MERGE COMPONENT 44, SPLITTER COMPONENT 42, FIG. 6B, 51 and 55 and related text).

As per claim 10, Tabloski, Jr. discloses the system of claim 1, at least one of said ports supporting multi-valued null data tokens (see at least col.9:45-65 "… any values provided by program developer…").

As per claim 12, Tabloski, Jr. discloses the system of claim 1, at least one of said map components being composite comprising a number of hierarchical dataflow graphs (see at least col.1:35-55 "… linked in a dataflow graph that represents the order of operations to be performed…").

As per claim 13, Tabloski, Jr. discloses the system of claim 1, the compiler operating to remove design time links between map components to produce a flat dataflow graph containing a plurality of map processes for execution (see at least e.g. FIG. 7, EXECUTION CONTROL

OBJECT 67 –"…to remove the block and enable the portion executable objects…" and related text).

As per claim 14, Tabloski, Jr. discloses the system of claim 1, the executor operating to assign a thread to each map process for parallel execution (see at least col.5:50-65 "… develop the parallel program graphically… instantiated program objects and links interconnecting respective objects to represent the flow of data…", e.g. FIG. 7A and related text).

As per claim 16, Tabloski, Jr. discloses a method of transforming data in parallel processing environment comprising a single operating system and one or more processors (see at least e.g. FIG. 1, FIG. 2, 25 and related text) wherein: map components are assembled visually into an integrated dataflow application by linking the map components and the integrated dataflow application is executed in parallel by recognizing the linked processes within the map components (see at least col.10:1-15 "… data flow… generate code for the object instances in the graph…", e.g. FIG. 2, EXECUTABLE PROGRAM 23 and FIG. 7A and related text) and allocating a thread to each process each map process is executed on its allocated thread substantially in parallel, and said data resides in memory accessible to each map process (see at least col.8:1-20 "… each be processed by a separate one … of the parallel computer system …", col.8:45-60 "… parallel processing… single instance of a parallel processing module can be processed in parallel on plurality of processors…" and e.g. FIG. 2, OUTPUT 24, FIG. 8, step 100 and related text).

As per claim 17, Tabloski, Jr. discloses the method of claim 16, wherein a plurality of map processes read data tokens from input ports and write data tokens to output ports (e.g. FIG. 2, OUTPUT 24, FIG. 8, step 100 and related text).

As per claim 18, Tabloski, Jr. discloses a method of managing data comprising: accessing a library of map components at least some of said map components constituting a specific data transformation and having input and output ports (e.g. FIG. 2, OUTPUT 24, FIG. 8, step 100 and related text) and tools for visually assembling map components into a dataflow application (see at least col.5:50-65 "… develop the parallel program graphically… instantiated program objects and links interconnecting respective objects to represent the flow of data…", e.g. FIG. 7A and related text); assembling a dataflow application using map components from said library linked together using said ports (see at least col.2:5-15 "… one or more input and/or output ports…. for receiving data from another component…", e.g. FIG. 6A, 41 and related text); and executing the assembled dataflow application with source data (see at least col.8:1-20 "… each be processed by a separate one … of the parallel computer system …", col.8:45-60 "… parallel processing… single instance of a parallel processing module can be processed in parallel on plurality of processors…" and e.g. FIG. 2, OUTPUT 24, FIG. 8, step 100 and related text).

As per claim 19, Tabloski, Jr. discloses the method of claim 18, including imposing properties on the map components during assembly constraining the assemblage of the dataflow application (see at least FIG. 8 PROGRAM COMPOSITION MODULE 33 TRAVERSES DATA FLOW GRAPH AND GENERATES HIGH-LEVEL LANGUAGE PROGRAM CODE and col.2:55-65 "… executable objects associated with … components… dataflow…").

As per claim 20, Tabloski, Jr. discloses the method of claim 18, the map components including polymorphic ports, which declare status as input and output ports during assemblage (e.g. FIG. 6A and 6B and related text).

As per claim 21, Tabloski, Jr. discloses the system of claim 14, the executor operating on a single CPU in a hyper thread architecture (e.g. FIG. 3 – "… splitter represented by the icon are to be partitioned among processors…" and related text).

As per claim 22, Tabloski, Jr. discloses the system of claim 14, the executor operating on a multiple processor core with at least some threads assigned to different processors (see at least col.4:30-45 "… parallel computers… a plurality of processors which communicate to transfer data and/or status…through network…").

As per claim 23, Tabloski, Jr. discloses the system of claim 14, the executor operating on multiple processors in a distributed network configuration (see at least col.4:30-45 "… parallel computers… a plurality of processors which communicate to transfer data and/or status…through network…",col.5:50-65 "… develop the parallel program graphically… instantiated program objects and links interconnecting respective objects to represent the flow of data…", e.g. FIG. 7A and related text.

As per claim 24, Tabloski, Jr. discloses the method of claim 16, communication between said processes executing in parallel being managed by an executor separate from the operating system (see at least col.8:1-20 "… each be processed by a separate one … of the parallel computer system …", col.8:45-60 "… parallel processing… single instance of a parallel processing module can be processed in parallel on plurality of processors…" and e.g. FIG. 2, OUTPUT 24, FIG. 8, step 100 and related text).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tabloski, Jr. et al (US 6,330,008 B1) in view in view of Wack et al. (US 7,095,852).

As per claim 11, Tabloski, Jr. does not explicitly disclose the system of claim 1, at least one of said map components being encoded as an encrypted extensible markup language (XML) document. However Wack discloses encryption schemes can be used to encrypt any type of data, encryption of XML data objects is of special interest, because XML's ability to capture the structure and semantics of data makes new applications available for cryptographic processes. Therefore it would have been obvious to one skilled in the art at the time of the invention was made to encrypt the map component to capture structure and semantics of data to create new dataflow graph as once suggested by Wack (col. 7:45-55).

8. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tabloski, Jr. et al (US 6,330,008 B1) in view of Yamanaka (US 6,993,753 B2).

As per claim 15, Tabloski, Jr. does not explicitly disclose the system of claim 1, the compiler tools operating to perform syntactic and semantic analysis, type inference and validation. However, Yamanaka discloses a compiler of Fig. 1, which performs syntactic and semantic analysis of a source program. Therefore it would have been obvious to one skilled in the art at the time the invention was made to perform semantic and syntactic analysis to process the verification process faster than in conventional method and to verify the hierarchical structure (map) as once suggested by Yamanaka (col. 1:45-55).

9. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tabloski, Jr. et al (US 6,330,008 B1) in view of Kakivaya et al. (US 7,124,405 B1).

As per claim 25, Tabloski, Jr. discloses substantially disclosed the invention as claimed above. However, Tabloski, Jr. was silent regarding the subject matter of determining if a port will block execution of thread; and avoiding a deadlock by allowing the data queue to grow at said determined port. Nevertheless, as evidenced by the teaching of Kakivaya, the subject matter of determining if a port will block execution of thread (see at least col.4:15-30, col.16:64-67 – col.17:1-10); and avoiding a deadlock by allowing the data queue to grow at said determined port (see at least col.4:5-25, col.10:10-35 and col.10:35-65) was known . Therefore, it would have been obvious to one of an ordinary skill in the art at the time the invention was made to have include the feature of in order to avoid latency by resolving any block of execution thread by the port which exacerbated in multi-threaded environment as once suggested by Kakivaya (see at least col.1:25-45).

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ISAAC T. TECKLU whose telephone number is (571) 272-7957. The examiner can normally be reached on M-TH 9:300A - 8:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Isaac T Tecklu/
Examiner, Art Unit 2192

/Tuan Q. Dam/
Supervisory Patent Examiner, Art Unit 2192